Amendments to the Claims

1. (Currently Amended) A semiconductor integrated circuit device comprising:

a first MOS transistor

having a first backgate region, a first conductive region, and a second conductive region, and

having the first backgate region and the first conductive region thereof connected together;

a second MOS transistor, of a same conductivity type as the first MOS transistor,

having a second backgate region, a third conductive region, and a fourth conductive region,

having the second backgate region and the third conductive region thereof connected to the first backgate region and the first conductive region of the first MOS transistor, and

receiving at the fourth conductive region thereof a first direct-current voltage;

a voltage setting circuit

setting a second direct-current voltage fed to a gate of the second MOS transistor; ~~and~~

an anti-reverse-current element

receiving the first direct-current voltage or a third direct-current voltage produced from the first direct-current voltage, and

connected to the voltage setting circuit in such a way as to prevent a reverse current from flowing through the voltage setting circuit; and

a feedback circuit

outputting to a gate of the first MOS transistor a value obtained by comparing a voltage at the second conductive region of the first MOS transistor with a reference voltage,

wherein the voltage setting circuit produces, according to the first direct-current voltage or the third direct-current voltage, the second direct-current voltage within a withstand voltage range of the second MOS transistor,

wherein a load is connected to ~~a connecting portion between the first conductive region of the first MOS transistor and the third conductive region of the second MOS transistor~~ the second conductive region of the first MOS transistor, and

wherein, between the first backgate region and the second conducting region of the first MOS transistor, a first parasitic diode is formed and, between the second backgate region and the fourth conducting region of the second MOS transistor, a second parasitic diode is formed.

2. (Cancelled)

3. (Original) A semiconductor integrated circuit device as clamed in claim 1, wherein the anti-reverse-current element is a diode.

4. (Original) A semiconductor integrated circuit device as clamed in claim 1,

wherein the voltage setting circuit is composed of voltage-division resistors.

5. (Currently Amended) A semiconductor integrated circuit device comprising:

a first MOS transistor of a P-channel type

including a backgate, a first P-type diffusion layer, and a second P-type diffusion layer, and

having the backgate and the first P-type diffusion layer thereof connected together;

a second MOS transistor of a P-channel type

having a backgate and a third P-type diffusion layer thereof connected to the backgate and the first P-type diffusion layer of the first MOS transistor, and

receiving at a fourth P-type diffusion layer thereof a first direct-current voltage;

a voltage-division resistor circuit

having one end thereof grounded, and

feeding, as a second direct-current voltage, a division voltage produced thereby to a gate of the second MOS transistor; ~~and~~

a diode

receiving at an anode thereof the first direct-current voltage or a third direct-current voltage produced from the first direct-current voltage, and

having a cathode thereof connected to another end of the voltage-division resistor circuit; and

an operational amplifier

receiving at a non-inverting input terminal thereof a voltage at the second P-type diffusion layer of the first MOS transistor,

receiving at an inverting input terminal thereof a reference voltage, and

outputting to a gate of the first MOS transistor a value obtained by comparing the voltage at the second P-type diffusion layer with the reference voltage,

wherein the second direct-current voltage from the voltage-division resistor circuit is kept within a withstand voltage range of the second MOS transistor according to the first direct-current voltage or the third direct-current voltage,

wherein a load is connected to ~~a connecting portion between the first P-type diffusion layer of the first MOS transistor and the third P-type diffusion layer of the second MOS transistor~~ the second P-type diffusion layer of the first MOS transistor, and

wherein, between the first backgate and the second P-type diffusion layer of the first MOS transistor, a first parasitic diode is formed and, between the second backgate and the fourth P-type diffusion layer of the second MOS transistor, a second parasitic diode is formed.

6. (Cancelled)

7. (Currently amended) A semiconductor integrated circuit device as claimed in claim 5, further comprising:

a constant current source that is connected to the second P-type diffusion layer of the first MOS transistor~~; and~~

~~an operational amplifier that receives, at a non-inverting input terminal thereof, a voltage at the second P-type diffusion layer of the first MOS transistor and that outputs to a gate of the first MOS transistor a value obtained by comparing the voltage at the second P-type diffusion layer with a reference voltage that the operational amplifier receives at an inverting input terminal thereof~~.